FAIRCHILD SEMICONDUCTOR®

December 2006

FM75
Low-Voltage Two-Wire Digital Temperature Sensor with Thermal Alarm

Features

- User Configurable to 9, 10, 11 or 12-bit Resolution
- Precision Calibrated to ±1°C, 0°C to 100°C Typical
- Temperature Range: -40°C to 125°C
- Low Operating Current (less than 250µA)
- Low Self Heating (0.2°C max. in still air)
- Operating Voltage Range: 2.7V to 5.5V

Applications

- Battery Management
- FAX Management
- Printers
- Portable Medical Instruments
- HVAC Systems
- Power Supply Modules
- Disk Drives
- Computers
- Automotive Components

Description

The FM75 contains a high-precision CMOS temperature sensor, a Delta-Sigma analog-to-digital converter, and a SMBus-compatible serial digital interface. Typical accuracy is ±2°C over the full temperature range of 40°C to 125°C and to ±1°C over the range of 0°C to 100°C, with 9- to 12-bit resolution (default is 9).

Thermal alarm output, over-limit signal (OS) supports interrupt and comparator modes. OS is active if the user-programmable trip-temperature is exceeded. When the temperature falls below the trip temperature, plus the user-programmable hysteresis limit, the OS is disabled.

Available in a surface mount SOIC-8 (SOP-8) package.

Application Diagram

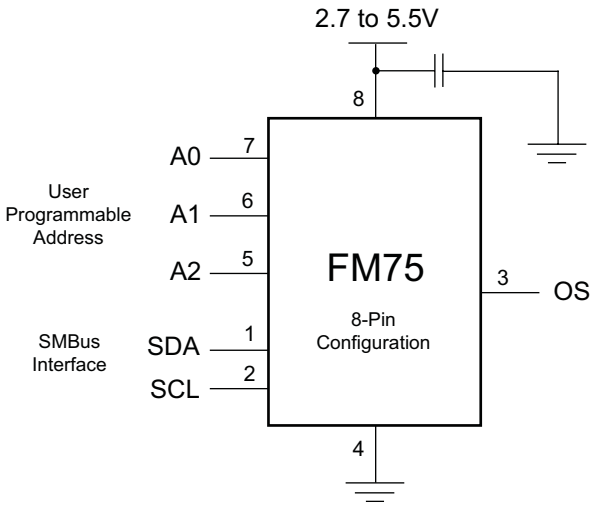


Figure 1. Typical Application Diagram

Ordering Information

Part Number	Package	Temperature Range	Packing Method
FM75M8x	8-Lead SOIC	-40°C to +125°C	2500 Units, Tape and Reel

Pin Assignments

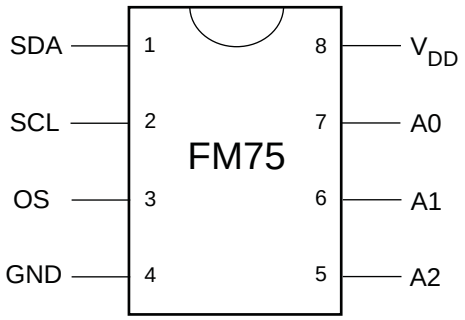


Figure 2. Pin Assignments

Pin Descriptions

Pin #	Name	Direction	Description
1	SDA	Input/Output	**Serial Data.** Open drain to I/O-data pin for two-wire interface.
2	SCL	Input	**Serial Clock.** Clock for two-wire serial interface.
3	OS	Output	**Over-Limit Signal.** Open drain thermostat output that indicates if the temperature exceeds user-programmable limits. Default is active LOW.
4	GND	Supply	Ground
5, 6, 7	A0, A1, A2	Input	**Address Least Significant Bits (LSBs).** User selectable address pins for the three LSBs of the serial interface address.
8	V_{DD}	Supply	Supply Voltage

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Parameter	Min.	Typ.	Max.	Units
Supply Voltage			+7	V
Output Voltage			V_{CC} + 0.5	V
Output Current			10	mA
Storage Temperature Range	-60		+150	°C
Lead Soldering Temperature			220	°C
ESD(1)				
Human Body Model			2000	V
Machine Model			250	V

Note:

1. Human Body Model: 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Machine Model: 200pF capacitor discharged directly into each pin.

Electrical Characteristics(2)

-40°C ð T_A ð +125°C, V_{CC} = 5.0V unless otherwise noted. Specifications are subject to change without notice.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{MIN}, T_{MAX}	Specified Temperature Range		-40		+125	°C
	Temperature Conversion Time(3)			90		ms
	Accuracy(4)	T_A = +25°C	-2		+2	°C
		T_A = +100°C	-3		+3	
		T_A = -40°C (T_{MIN})	-4		+4	
		T_A = +125°C (T_{MAX})	-4		+4	

Notes:

2. These specifications are guaranteed only for the test conditions listed.
3. This specification only indicates how often temperature information is updated to the temperature register. The FM75 can be read at any time without interrupting the temperature conversion process.
4. Accuracy (expressed in °C) = the difference between the FM75 output temperature and the measured temperature.

Logic Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Minimum Input Voltage Logic HIGH		V_{DD} x 0.7		V_{DD} + 0.5	V
V_{IL}	Maximum Input Voltage Logic LOW		-0.3		V_{DD} x 0.3	V
V_{OL}	Maximum Output Voltage Logic LOW	V_{DD} = 5V, I_{OL} = -3mA V_{DD} = 3V, I_{OL} = -1.5mA			0.36 0.36	V V
I_{DD}	Quiescent Supply Current	Interface Inactive R/W Activity on SDA		250 350	500 700	µA
I_{DD-SD}	Shutdown Current	Interface Inactive R/W Activity on SDA		0.15 83	1 150	µA
I_{IN}	Input Leakage Current	V_{IN} = 0V or 5V, T_A = 25°C -40°C < T_A < 125°C			±0.1 ±1.0	µA
I_{OL}	Output Sink Current	T_A = 25°C, V_{OL} = 0.4V			3	mA
I_{LEAK}	Output Leakage Current	V_{OH} = 5V, V_{DD} = 0V		0.001	5	µA
t_F	Output Transition Time	C_L = 400pF, I_{OL} = -3mA			250	ns
C_{IN}	Input Capacitance	All Digital Inputs			20	pF

Serial Port Timing

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{SCL}	SCL Clock Period		1.0		100	µs
$t_{T:LH}$, $t_{T:HL}$	SCL Clock Transition Time				300	ns
t_{LOW}	SCL Clock LOW Period		0.470			µs
t_{HIGH}	SCL Clock HIGH Period		0.400		50	µs
t_{BUF}	Bus free time between a Stop and a new Start Condition		1.0			µs
$t_{SU:DAT}$	Data In Set-up to SCL HIGH		100			ns
$t_{HD:DAT}$	Data In Hold Time		100			ns
t_{HD}	Data Out Stable after SCL LOW		0			ns
$t_{SU:STA}$	SCL LOW Set-up to SDA LOW (Repeated Start Condition)		100			ns
$t_{HD:STA}$	SCL HIGH Hold after SDA LOW (Start Condition)		100			ns
$t_{SU:STO}$	SDA HIGH after SCL HIGH (Stop Condition)		100			ns
t_{POR}	Time in which a FM75 must be operational after a power-on reset				500	ms

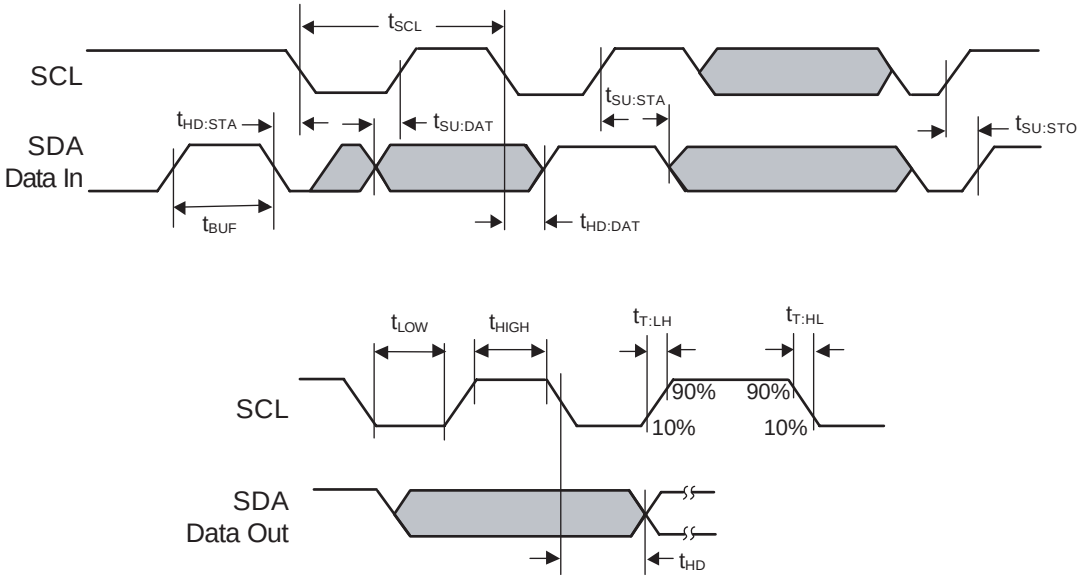


Figure 3. Serial Port Timing Diagram

Basic Operation

The FM75 temperature sensing circuitry continuously produces analog voltage proportional to the device temperature. At regular intervals, the FM75 converts the analog voltage to a two's complement digital value, which is placed into the temperature register.

The FM75 has an SMBus-compatible digital serial interface that allows access to the data in the temperature register at any time. In addition, the serial interface provides access to all other FM75 registers to customize operation of the device.

The FM75 temperature-to-digital conversion can have 9, 10, 11, or 12-bit resolution selected, providing 0.5°C, 0.25°C, 0.125°C, and 0.0625°C temperature resolution, respectively. At power-up, the default conversion resolution is 9-bits. The conversion resolution is controlled by the R0 and R1 bits in the configuration register.

Table 1 gives examples of the relationship between the output digital data and the external temperature. The 9-bit, 10-bit, 11-bit, and 12-bit columns in Table 1 indicate the right-most bit in the output data stream that can contain temperature information for each conversion accuracy. Since the output digital data is in two's-complement format, the most significant bit of the temperature is the "sign" bit. If the sign bit is zero, the temperature is positive; if the sign bit is one, the temperature is negative.

The FM75 has a shutdown mode that reduces the operating current to 150nA. This mode is controlled by the SD bit in the configuration register.

Power-Up Default Conditions

The FM75 powers up in the following default state:

- Thermostat mode: comparator mode
- OS polarity: active LOW
- Fault tolerance: 1 fault (i.e., F0 = 0 and F1 = 0 in the configuration register)
- T_{OS}: 80°C
- T_{HYST}: 75°C
- Register pointer: 00 (temperature register)
- Conversion resolution: 9 bits (i.e., R0 = 0 and R1 = 0 in the configuration register)

After power-up, these conditions can be reprogrammed via the serial interface. Refer to the *Serial Data Bus Operation* section for FM75 programming instructions.

Thermal Alarm Function

The FM75 thermal alarm function provides programmable thermostat capability and allows the FM75 to function as a stand-alone thermostat without using the serial interface. The Over-Limit Signal (OS) output is the alarm output. This signal is an open-drain output and, at power-up, this pin is configured with active-low polarity.

Table 1. Relationship Between Temperature and Digital Output

Temperature	Digital Output							
	Sig	Number of bits used by conversion resolution		bit 9	bit 10	bit 11	bit 12	Always zero
All Temperatures	12-Bit Resolution							0000
	11-Bit Resolution						0	0000
	10-Bit Resolution					0	0	0000
	9-Bit Resolution				0	0	0	0000
+125 C	0	111	1101	0	0	0	0	0000
+100.0625 C	0	110	0100	0	0	0	1	0000
+50.125 C	0	011	0010	0	0	1	0	0000
+12.25 C	0	000	1100	0	1	0	0	0000
0 C	0	000	0000	0	0	0	0	0000
-20.5 C	1	110	1011	1	0	0	0	0000
-33.25C	1	101	1110	1	1	0	0	0000
-45.0625 C	1	101	0010	1	1	1	1	0000
-55C	1	100	1001	0	0	0	0	0000

The OS polarity is controlled by the POL bit in the configuration register. The programmable upper trip-point temperature for the thermal alarm is stored in the T_{OS} register. The programmable hysteresis temperature (i.e., the lower trip point) is stored in the T_{HYST} register.

The thermal alarm has two modes of operation: comparator mode and interrupt mode. At power-up, the default is comparator mode. The alarm mode is controlled by the CMP/INTR bit in the configuration register.

Fault Tolerance

For both comparator and Interrupt modes, the alarm "fault tolerance" setting plays a role in determining when the OS output is activated. Fault tolerance refers to the number of consecutive times an error condition must be detected before the user is notified. Higher fault tolerance settings can help eliminate false alarms caused by noise in the system. The alarm fault tolerance is controlled by bits F0 and F1 in the configuration register. These bits can be used to set the fault tolerance to 1, 2, 4, or 6, as shown in Table 4. At power-up, these bits both default to 0 (fault tolerance = 1).

Comparator Mode

In comparator mode, each time a temperature-to-digital (T-to-D) temperature conversion occurs, the new digital temperature is compared to the value stored in the T_{OS} and T_{HYST} registers. If a fault tolerance number of consecutive temperature measurements are greater than the value stored in the T_{OS} register, the OS output is activated. For example, if bits F1 and F0 are equal to "10" (fault tolerance = 4), four consecutive temperature measurements must exceed T_{OS} to activate the OS output. Once the OS output is active, it remains active until the first time the measured temperature drops below the temperature stored in the T_{HYST} register. The operation of the alarm in comparator mode with fault tolerance = 2 is illustrated in Figure 4.

Interrupt Mode

In interrupt mode, the OS output first becomes active after a fault tolerance number of consecutive temperature measurements exceed the value stored in the T_{OS} register (similar to comparator mode). Once OS is active, it can only be cleared by a user read from any of the FM75 registers (temperature, configuration, T_{OS}, or T_{HYST}) or by putting the FM75 into shutdown mode (i.e., by setting the shutdown bit in the configuration register to "1"). Once cleared, the OS output can only be activated the next time by a fault tolerance number of consecutive temperature measurements lower than the value stored in T_{HYST}. Once it is activated, the OS output can only be deactivated by a user read or shutdown. In interrupt mode, the activate/clear cycle for OS has the following pattern: temperature > T_{OS}, clear, temperature < T_{HYST}, clear, temperature > T_{OS}, clear, etc. The operation of the alarm in interrupt mode with fault tolerance = 2 is illustrated in Figure 4.

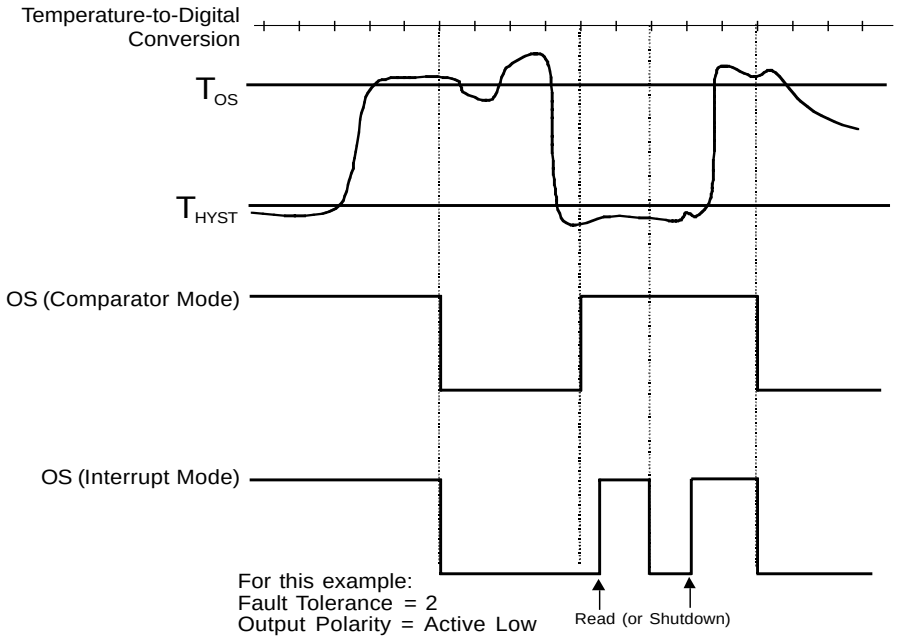


Figure 4. Thermal Alarm Operation in Comparator and Interrupt Modes

Registers

The FM75 contains the following five registers:

- Command Register
- Temperature Register
- Configuration Register
- Over-Limit-Signal Temperature Register (T_{OS})
- Hysteresis Temperature Register (T_{HYST})

All of these registers can be accessed by the user via the digital serial interface at any time *(see Serial Interface Operation for instructions)*. A detailed description of these registers and their functions is provided in the following sections. A diagram of the register hierarchy is shown in Figure 5.

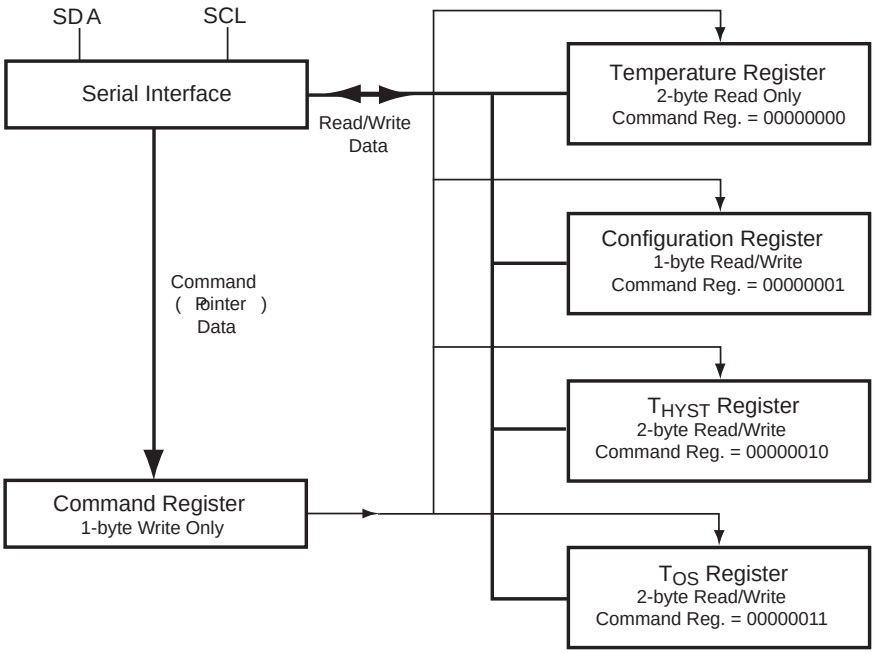


Figure 5. Register Hierarchy

Command Register

The command register is a one-byte (8-bit) write-only register. The data stored in the command register indicates which of the other registers (temperature, configuration, T_{OS}, or T_{HYST}) to read from or write to during an upcoming operation. The command register "points" to the selected register, as shown in Figure 11.

The command register is illustrated in Figure 9. The P1 and P0 bits of the command register determine which register is accessed, as shown in Table 2. The six Most Significant Bits (MSBs) of the command register must always be zero. Writing a one into any of these bits causes the current operation to be terminated.

The command register retains pointer information between operations; therefore, this register only needs to be updated once for consecutive read operations from the same register. All bits in the command register default to zero at power-up.

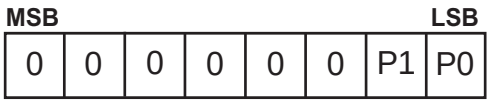


Figure 6. Command Register Format

Table 2. Register Assignments for Command Bits P1 and P2

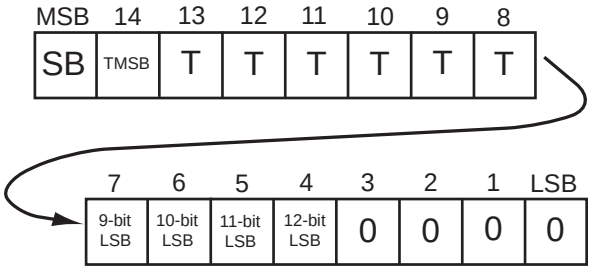
Register	P1	P0
Temperature Register	0	0
Configuration Register	0	1
T_{HYST} Register	1	0
T_{OS} Register	1	1

Temperature Register

The temperature register is a two-byte (16-bit) read-only register. Digital temperatures from the T-to-D converter are stored in the temperature register in two's complement format and the contents of this register are updated at regular intervals, each time the T-to-D conversion is finished.

The user can read data from the temperature register at any time. When a T-to-D conversion is completed, the new data is loaded into a comparator buffer to evaluate fault conditions and updates the temperature register if a read cycle is not ongoing. The FM75 is continuously evaluating fault conditions regardless of read or write activity on the bus. If a read is ongoing, the previous temperature is read. The readable temperature is updated upon the completion of the next T-to-D conversion not masked by a read cycle.

The temperature register is illustrated in Figure 7. Depending on the resolution of the T-to-D conversion, the 9, 10, 11, or 12 MSBs of the register contain temperature data. All unused bits following the digital temperature are zero. The MSB position of the temperature register always contains the sign bit for the digital temperature and bit 14 contains the temperature MSB. Bits in the temperature register default to zero at power-up.

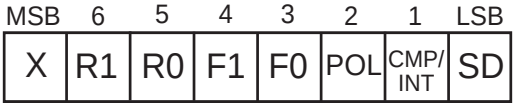


SB = Two's complement sign bit
TMSB = Temperature MSB
T = Temperature data
9-bit LSB = Temperature LSB for 9-bit conversions
10-bit LSB = Temperature LSB for 10-bit conversions
11-bit LSB = Temperature LSB for 11-bit conversions
12-bit LSB = Temperature LSB for 12-bit conversions

Figure 7. Temperature Register Format

Configuration Register

The configuration register is a one-byte (8-bit) read/write register (see Figure 8). This register allows the user to control the FM75 shutdown mode as well as the following thermal alarm features: polarity, operating mode, and fault tolerance. The configuration register contains two bits that set the fault tolerance trip point. The fault tolerance trip point is the number of consecutive times the internal circuit reads the temperature and finds the temperature outside the limits programmed. The programmed limits are defined by the T_{OS} register for the upper limit and by the T_{HYST} register for the lower limit. Table 4 shows the relationship between F1 and F0 and the number of consecutive errors or "trips" needed to activate the alarm. The configuration register also contains the two bits that set the T-to-D conversion resolution to 9, 10, 11, or 12 bits. Table 3 shows the relationship between R1 and T0 and the conversion resolution. All bits in the configuration register default to zero at power-up.



R1 = Resolution bit 1 (see Table 3).
R0 = Resolution bit 0 (see Table 3).
F1 = Fault tolerance bit 1 (see Table 4).
F0 = Fault tolerance bit 0 (see Table 4).
POL = OS output polarity: 0 = active low, 1 = active high.
CMP/INT = thermostat mode: 0 = comparator mode, 1 = inerrupt mode.
SD = shutdown: 0 = normal operation, 1 = shutdown mode.

Figure 8. Configuration Register Format

Table 3. Conversion Resolution Settings

A-to-D Conversion Resolution	R1	R0
9 Bits	0	0
10 Bits	0	1
11 Bits	1	0
12 Bits	1	1

Table 4. Fault Tolerance Settings

Fault Tolerance	R1	R0
1	0	0
2	0	1
4	1	0
6	1	1

Over-Limit Signal Temperature Register (T_{OS})

The T_{OS} register is a two-byte (16-bit) read/write register that stores the user-programmable upper trip-point temperature for the thermal alarm in two's-complement format. At power-up, this register defaults to 80°C (i.e. 0101 0000 0000 0000).

The format of the T_{OS} register is identical to that of the temperature register (see Figure 9). The four LSBs of the T_{OS} register are hardwired to zero, so data written to these register bits is ignored. The MSB position of the T_{OS} register contains the sign bit for the digital temperature and bit 14 contains the temperature MSB.

The resolution setting for the T-to-D conversion determines how many bits of the T_{OS} register are used by the thermal alarm. For example, for 9-bit conversions, the trip-point temperature is defined by the nine MSBs of the T_{OS} register and all remaining bits are ignored.

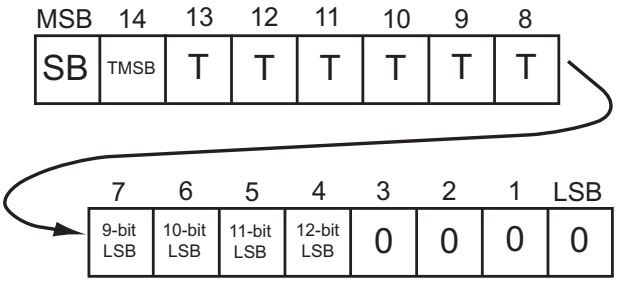
Hysteresis Temperature Register (T_{HYST})

The T_{HYST} register is a two-byte (16-bit) read/write register that stores the programmable lower trip-point temperature for the thermal alarm in two's-complement format. At power-up, this register defaults to 75°C (i.e. 0100 1011 0000 0000).

The T_{HYST} register is illustrated in Figure 9. The format of this register is the same as that of the temperature register. The four LSBs of the T_{HYST} register are hardwired to zero, so data written to these bits is ignored.

The resolution setting for the T-to-D conversion determines how many bits of the T_{HYST} register are used by the thermal alarm. For example, for 9-bit conversions, the hysteresis temperature is defined by the nine MSBs of the T_{HYST} register and all remaining bits are ignored.

.



SB = Two's complement sign bit
TMSB = Temperature MSB
T = Temperature data
9-bit LSB = Temperature LSB for 9-bit conversions
10-bit LSB = Temperature LSB for 10-bit conversions
11-bit LSB = Temperature LSB for 11-bit conversions
12-bit LSB = Temperature LSB for 12-bit conversions

Figure 9. T_{HYST} Register and T_{OS} Register Format

Serial Data Bus Operation

General Operation

Writing to and reading from the FM75 registers is accomplished via the SMBus-compatible two-wire serial interface. SMBus protocol requires that one device on the bus initiates and controls all read and write operations. This device is called the “master” device. The master device also generates the SCL signal, which is the clock signal for all other devices on the bus. All other devices on the bus are called “slave” devices. The FM75 is a slave device. Both the master and slave devices can send and receive data on the bus.

During SMBus operations, one data bit is transmitted per clock cycle. All SMBus operations follow a repeating nine clock-cycle pattern that consists of eight bits (one byte) of transmitted data followed by an acknowledge (ACK) or not acknowledge (NACK) from the receiving device. Note that there are no unused clock cycles during any operation—therefore there must be no breaks in the stream of data and ACKs/NACKs during data transfers. Conversely, too few clock cycles can lead to incorrect operation if an inadvertent 8-bit read from a 16-bit register occurs.

For most operations, SMBus protocol requires the SDA line to remain stable (unmoving) whenever SCL is HIGH—i.e., transitions on the SDA line can only occur when SCL is LOW. The exceptions to this rule are when the master device issues a start or stop signal. The slave device cannot issue a start or stop signal.

Start Condition: This condition occurs when the SDA line transitions from HIGH to LOW while SCL is HIGH. The master device uses this condition to indicate that a data transfer is about to begin.

Stop Condition: This condition occurs when the SDA line transitions from LOW to HIGH while SCL is HIGH. The master device uses this condition to signal the end of a data transfer.

Acknowledge and **Not Acknowledge:** When data is transferred to the slave device, it sends an acknowledge (ACK) after receiving every byte of data. A master device sends an acknowledge (ACK) following only the first byte read from a two-byte register. The receiving device sends an ACK by pulling SDA LOW for one clock cycle. Following the last byte, a master device sends a “not acknowledge” (NACK) followed by a stop condition. A NACK is indicated by leaving SDA HIGH during the clock after the last byte.

Slave Address

Each slave device on the bus has a unique 7-bit address so the master can identify which device is sending or receiving data.

The FM75 address is as follows:

1	0	0	1	A2	A1	A0

The four MSBs of the FM75 address are hardwired to 1001. The three LSBs are user configurable by tying the A0, A1, and A2 pins to either V_{DD} or ground. This provides eight different FM75 addresses, which allows up to eight FM75s to be connected to the same bus.

Writing to and Reading from the FM75

All read and write operations must begin with a start signal generated by the master device. After the start condition, the master device must immediately send a slave address (7 bits), followed by a read/write bit. If the slave address matches the address of the FM75, the FM75 sends an ACK after receiving the read/write bit by pulling the SDA line LOW for one clock cycle. Figures 11 -16 provide timing diagrams for all FM75 operations.

Setting the Pointer

For all operations, the pointer stored in the command register must be pointing to the register (temperature, configuration, T_{OS} or T_{HYST}) that is going to be written to or read from. To change the pointer value in the command register, the read/write bit following the address must be 0. This indicates that the master will write new information into the command register.

After the FM75 sends an ACK in response to receiving the address and read/write bit, the master device must transmit an appropriate 8-bit pointer value, as explained in the *Registers* section. The FM75 sends an ACK after receiving the new pointer data.

The pointer set operation is illustrated in Figure 11. Anytime a pointer set is performed, it must be immediately followed by a read or write operation. Note that the six MSBs of the pointer value must be zero. If the six MSBs are not zero, the FM75 does not send an ACK and internally terminates the operation. The command register retains the current pointer value between operations; therefore, once a register is indicated, subsequent read operations do not require a pointer set cycle. Write operations always require the pointer be reset.

Reading

If the pointer is already pointing to the desired register, the master can read from that register by setting the read/write bit (following the slave address) to a one. After sending an ACK, the FM75 begins transmitting data during the following clock cycle. If the configuration register is being read, the FM75 transmits one byte of data (see Figure 13). The master should respond with a NACK, followed by a stop condition. If the temperature, $T_{OS,}$ or T_{HYST} register is being read, the FM75 transmits two bytes of data (see Figure 12). The master must respond to the first byte of data with an ACK and to the second byte of data with a NACK followed by a stop condition.

To read from a register other than the one currently indicated by the command register, a pointer to the desired register must be set. Immediately following the pointer set, the master must perform a repeat start condition (see Figure 11 and Figure 15), which indicates to the FM75 that a new operation is about to occur. If the repeat start condition does not occur, the FM75 assumes that a write is taking place and the selected register is overwritten by the upcoming data on the data bus. After the start condition, the master must again send the device address and read/write bit. This time, the read/write bit must be set to one to indicate a read. The rest of the read cycle is the same as described in the previous paragraph for reading from a preset pointer location.

Writing

All writes must be proceeded by a pointer set, even if the pointer is already pointing to the desired register.

Immediately following the pointer set, the master must begin transmitting the data to be written. If the master is writing to the configuration register, one byte of data must be sent (see Figure 16). If the T_{OS} or T_{HYST} register is being written, the master must send two bytes of data (see Figure 14). After transmitting each byte of data, the master must release the Serial Data (SDA) line for one clock cycle to allow the FM75 to acknowledge receiving the byte. The write operation should be terminated by a stop signal from the master.

Caution: Inadvertent 8-Bit Read from a 16-Bit Register

An inadvertent 8-bit read from a 16-bit register, with the D7 bit LOW, can cause the FM75 to pause in a state where the SDA line is pulled LOW by the output data and is incapable of receiving either a stop or a start condition from the master. The only way to remove the FM75 from this state is to continue clocking for nine cycles until SDA goes HIGH, at which time issuing a stop condition resets the FM75, shown in Figure 10.

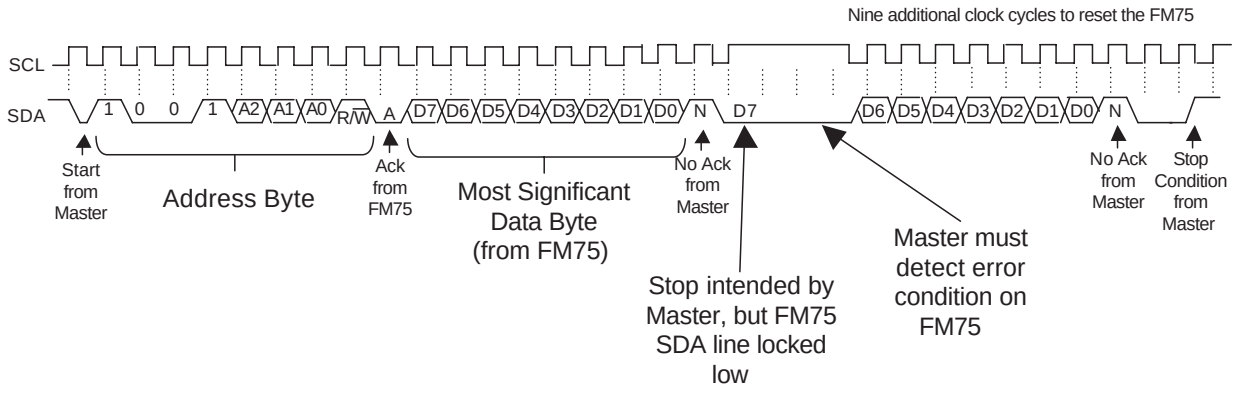


Figure 10. Inadvertent 8-Bit Read from 16-Bit Register Where D7 = 0 and Forces Output LOW

Timing Diagrams

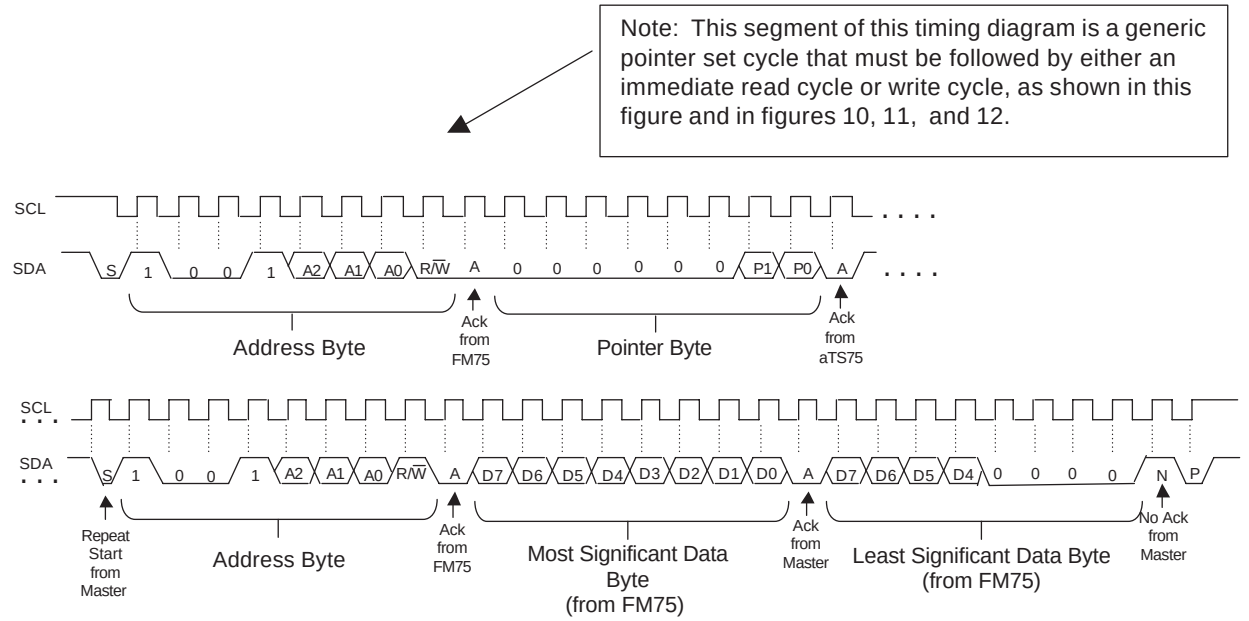


Figure 11. Pointer Set Followed by Immediate Read from a Two-byte Register (Temperature, T_{OS}, or T_{HYST} Register)

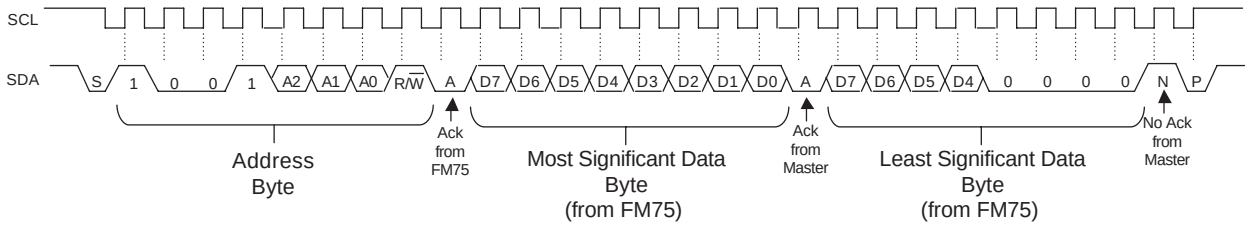


Figure 12. Two-byte Read from Preset Pointer Location (Temperature, T_{OS}, or T_{HYST} Register)

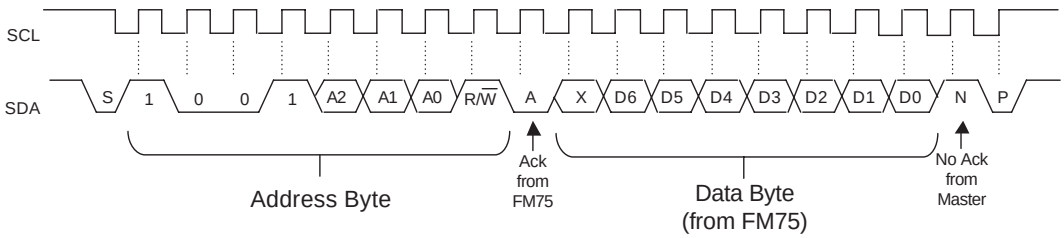


Figure 13. One-byte Read from Configuration Register with Preset Pointer

Timing Diagrams (Continued)

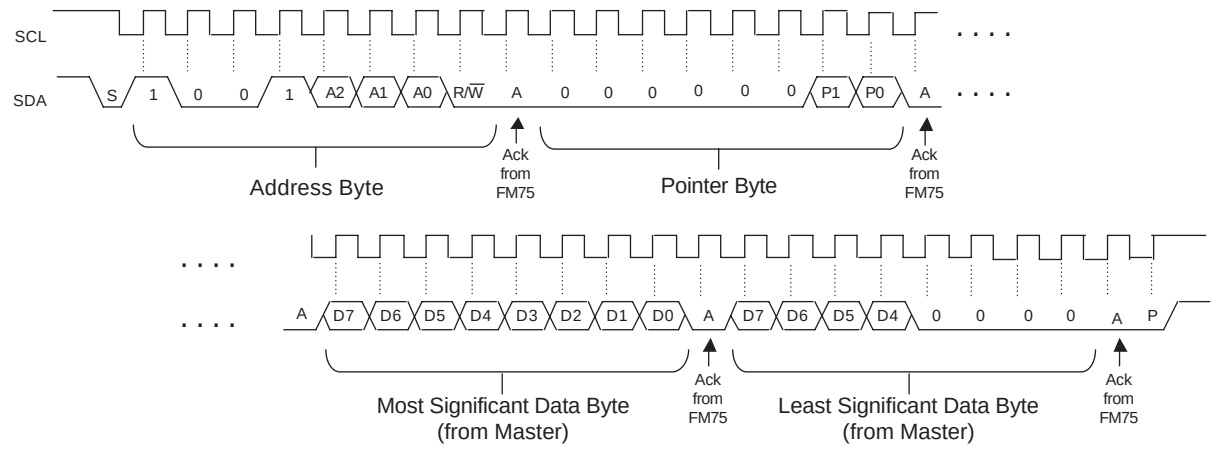


Figure 14. Pointer Set Followed by Immediate Write to A 2-byte Register (T_{OS} or T_{HYST} Register)

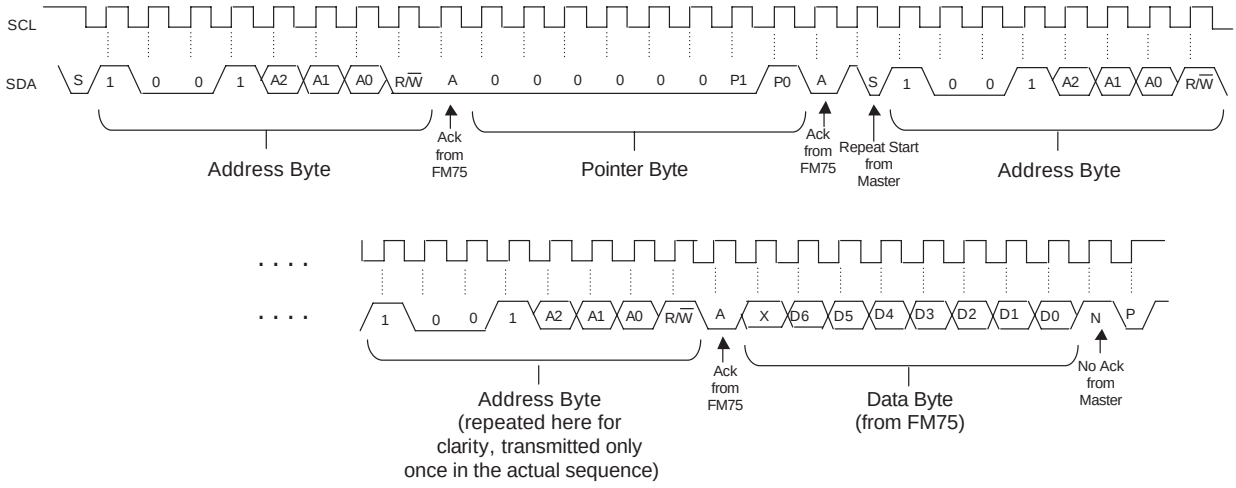


Figure 15. Pointer Set Followed by Immediate Read from Configuration Register

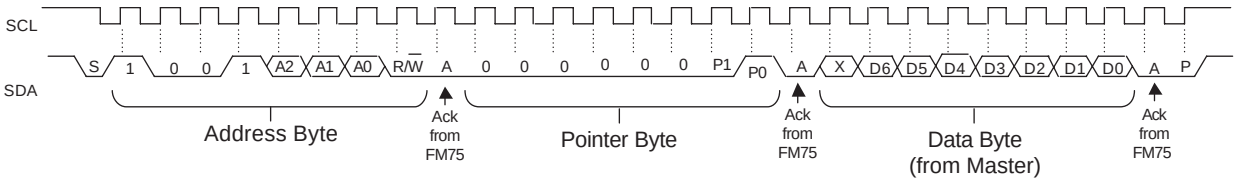


Figure 16. Pointer Set Followed by Immediate Write to the Configuration Register

Mechanical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

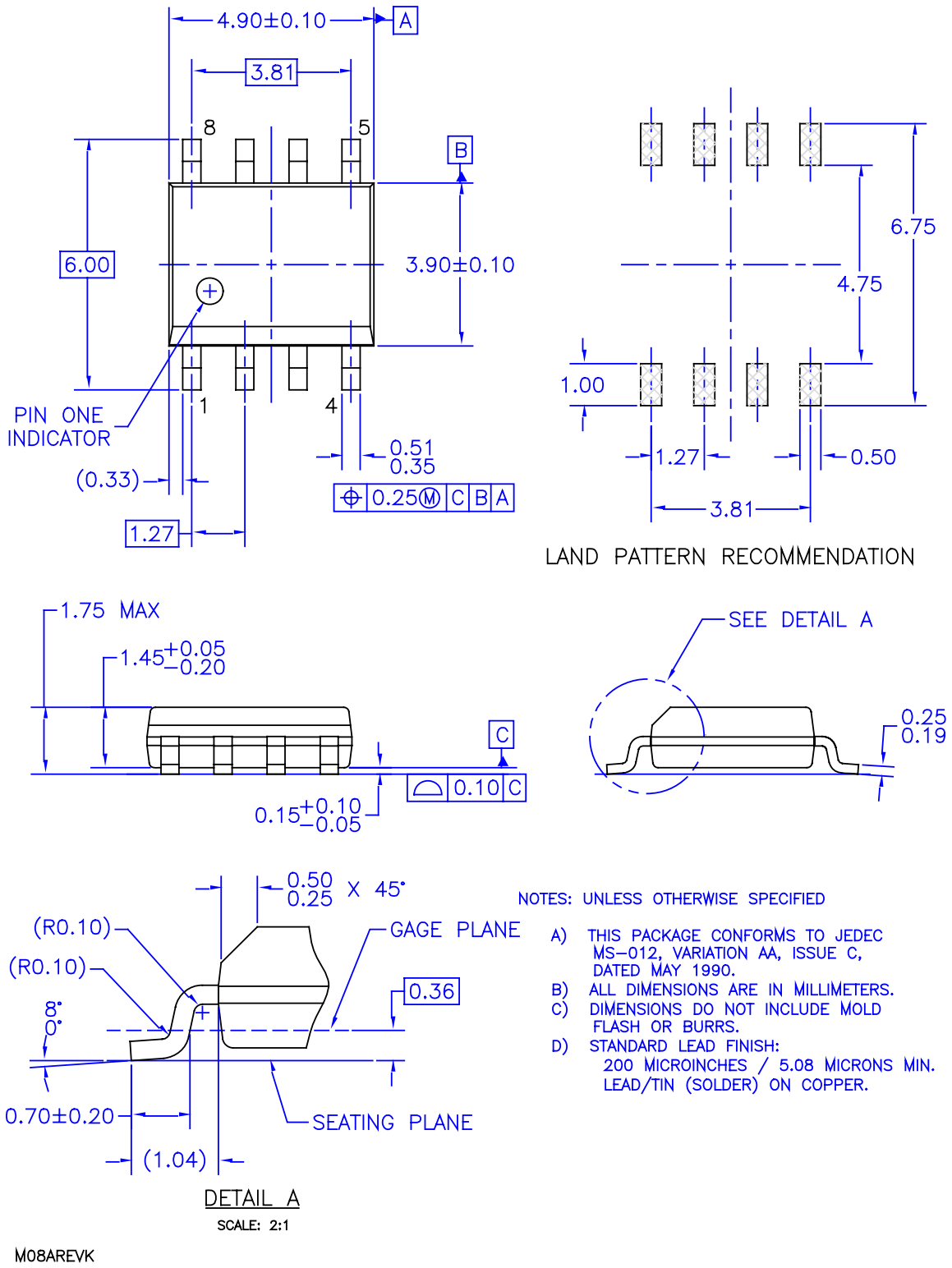


Figure 17. Molded Package, Small Outline, 0.15 Wide, 8-Lead (M8)

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FACT Quiet Series™	OCX™	SILENT SWITCHER®	UniFET™
ActiveArray™	GlobalOptoisolator™	OCXPro™	SMART START™	VCX™
Bottomless™	GTO™	OPTOLOGIC®	SPM™	Wire™
Build it Now™	HiSeC™	OPTOPLANAR™	Stealth™	
CoolFET™	I^2C™	PACMAN™	SuperFET™	
CROSSVOLT™	*i-Lo*™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™-6	
EcoSPARK™	IntelliMAX™	PowerEdge™	SuperSOT™-8	
E^2CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT®	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
Across the board. Around the world.™		µSerDes™	TruTranslation™	
The Power Franchise®		ScalarPump™	UHC®	
Programmable Active Droop™				

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I22